REMARKS

Claims 1-4, 6-17 and 20-33 stand rejected under 35 U.S.C. 102(b). Claims 5, 18-19 were cancelled in Applicants' previously-filed response.[1] Applicants have amended claim 7 to remove a grammatical irregularity. Claims 1-4, 6-17 and 20-33 remain pending. The Examiner's bases for rejecting those claims are addressed below. Reconsideration of the application is respectfully requested.

Rejections Under 35 U.S.C. 102(b)

The Examiner rejected claims 1-4, 6-17 and 20-33 under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,698,869 to Yoshimi et al.[2] Yoshimi et al. describes a prior art fabrication process for a particular generation of field effect transistors called a SOLMOSFET in which a silicon-germanium region 207 is formed in a silicon substrate, preferably entirely within the interior of a source drain region 206. The silicon germanium layer 207 is not a buried region in that it extends from the surface of the silicon substrate down to some depth in the silicon body as shown in FIG. 4A. While FIG. 4A of Yoshimi et al. shows the desired processing outcome, FIG. 7 depicts, at least in the eyes of the Yoshimi et al. inventors, an example of unsuccessful processing. In particular, FIG. 7 shows an example of what might happen if the silicon-germanium region 207 is formed with its lateral boundary too close to the source/drain region junction interface 215. According to Yoshimi et al., a crystal defect region, D, is generated so as to traverse the pn junction interface 215 of the source/drain region 206 and the channel region 203. The crystal defect region D consists of multiple, parallel defect planes generated mainly along the {111} planes.

Claim 1 recites, *inter alia*, forming a buried amorphous region in a device region and forming a dislocation region in the device region by annealing the substrate to recrystallize the

---

[1]Response to the Office Action Mailed September 25, 2003, filed on October 9, 2003.

[2]The element numbering used in Yoshimi et al. is followed herein.

buried amorphous region. The Examiner is directed to FIGS. 6 and 7 of Applicants' drawings. Therein is depicted formation of a buried amorphous region 88.[3]

It may be helpful to now directly contrast the exemplary buried amorphous region 88 with the silicon germanium film 207 cited by the Examiner. The silicon germanium film 207 in FIG. 7 of Yoshimi et al. is a surface film extending from the surface of the silicon down to some depth in the body thereof. It is thus, by definition, not a buried amorphous region.

The foregoing discussion is directed primarily to claim 1 and the claims depending therefrom. Applicants now take this opportunity to comment specifically on the rejection of various other claims.

Claim 2 is distinguishable over Yoshimi et al. for the reasons advanced above for claim 1.

Claim 3 is distinguishable over Yoshimi et al. for the reasons advanced above for claim 2.

Claim 4 is distinguishable over the teachings of Yoshimi et al. for the reasons advanced above with regard to claim 1.

Claim 6 is distinguishable over Yoshimi et al. for the reasons advanced above for claim 1.

Claim 7 recites, *inter alia*, the formation of a buried amorphous region in the device region and the formation of one of two dislocation regions by annealing the substrate to recrystallize the buried amorphous region. Thus, for reasons similar to those advanced above with regard to claim 1, claim 7 is distinguishable over Yoshimi et al.

Claims 8, 9, 10 and 11 are distinguishable over the teachings of Yoshimi et al. for the same general reasons advanced above with regard to claims 2 and 3, albeit in the context of the base claim 7.

Claim 12 is distinguishable over Yoshimi et al. since Yoshimi et al. does not disclose the formation of two buried amorphous regions and a dislocation region traversing a junction.

Claim 13 is distinguishable over Yoshimi et al. for the reasons advanced above with regard to claim 12.

---

[3]Of course, FIGS. 6 and 7 show the formation of buried amorphous regions 90, 106 and 108 as well.

Claim 14 recites, *inter alia*, the forming of first and second buried amorphous regions and the forming of first and second dislocation regions by recrystallizing the first and second buried amorphous regions. As noted above in the discussion of claim 1, Yoshimi et al. does not disclose the formation of buried amorphous regions or the formation of dislocation regions traversing a junction from those amorphous regions.

Claims 15 and 16 are distinguishable over Yoshimi et al. for the reasons generally advanced above with regard to claims 2 and 3, albeit in the context of base claim 14.

Claim 17 is distinguishable over Yoshimi et al. for the reasons advanced above with regard to claims 15 and 16.

For the reasons advanced above with regard to the patentability of claim 14, Applicants submit that claim 20 is similarly distinguishable over Yoshimi et al.

Claim 21 recites, *inter alia*, formation of first and second dislocation regions in a device region wherein the first and second dislocation regions are in non-parallel spatial relationship and traverse a junction. The Examiner is directed to the non-parallel dislocation regions 60 and 64 in FIG. 2 of Applicants' drawings. The features identified in Yoshimi et al. as crystal defects in FIG. 7 are parallel in space.

Claims 22, 23 and 24 are distinguishable over Yoshimi et al. for the reasons generally advanced above with regard to claims 2 and 3, albeit in the context of base claim 21. Claims 25, 26 and 27 are distinguishable over the teachings of Yoshimi et al. for the reasons advanced above with regard to claim 21.

Applicants respectfully take this opportunity to point out to the Examiner that claim 28 recites, *inter alia*, first and second impurity regions with respective first and second extension regions. An exemplary extension region 46 is shown in FIG. 2 of Applicants' drawings. Note that a dislocation region 60 traverses the junction 56. The Examiner has again cited the structure in FIG. 7 of Yoshimi et al. However, the region 206 in Yoshimi et al. is not a source/drain extension region. Thus, FIG. 7 and the accompanying text of Yoshimi et al. do not disclose a device including source/drain extension regions and dislocation regions traversing the junctions of those source/drain regions. Applicants do point out that FIG. 17B of Yoshimi et al. appears to disclose a structure 285

that is akin to a source/drain extension region. However, the dislocation D does not traverse the junction of the structure 285.

Applicants submit that claims 29-33 are similarly distinguishable over Yoshimi et al. for the reasons advanced above with regard to claim 28.

Conclusion

For the extensive reasons advanced above, Applicants submit that claims 1-4, 6-17 and 20-33 are patentable and respectfully request that a Notice of Allowability issue in due course.

Interview Summary

The Examiner graciously granted a telephone interview on January 27, 2004. During the interview, the undersigned and the Examiner discussed claim 1 and the undersigned presented the argument as generally outlined above directed to claim 1 and Yoshimi et al. The Examiner invited the submission of this paper.

Miscellaneous

The Assistant Commissioner is authorized to charge any required fees or credit any overpayment to Deposit Account No. 01-0365, Order No. AMDI:115\HON.

Respectfully submitted,

Date: January 29, 2004

Timothy M. Honeycutt
Reg. No. 37,153
Attorney at Law
P.O. Box 1577
Cypress, Texas 77410-1577
(281) 379-7999 Voice
(281) 379-7997 Fax
timhoney@sprynet.com e-mail
Attorney for Assignee
ADVANCED MICRO DEVICES, INC.